buffers the large stress inherent silicon nitride layer 324 and provides an etch step for silicon nitride layer 324 during a subsequent spacer etch.

Next, silicon nitride layer 324, and oxide layer 322, are anisotropically etched to form a pair of composite spacers 326 adjacent to the first pair of silicon nitride spacers 310 as shown in Figure 9. Any well known silicon nitride and oxide etchant process may be used to anisotropically etch silicon nitride layer 324 and buffer oxide layer 322. Additionally, it is to be appreciated that although composite spacers are utilized a single nitride or oxide layer can be used to form spacers 326 if desired. Spacers 326 are used to separate a silicide on the source/drain regions from a silicide on the gate region and/or to offset a high energy high dose implant from the active channel region. In an embodiment of the present invention spacers 326 have a thickness between 500-2000Å.

IN THE CLAIMS

Presented below are the amended claims in a clean-unmarked format.

1. (Amended) An MOS device comprising:

a gate dielectric formed on first conductivity region in a substrate;

a gate electrode formed on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and

a pair of deposited silicon or silicon alloy source/drain regions of a second conductivity type formed in said substrate and on opposite sides of said gate electrode, wherein said silicon or silicon alloy source/drain regions extend beneath the gate electrode and define a channel region beneath said gate electrode in said first conductivity type region, and wherein said channel region directly beneath said gate

electrode is larger than said channel region deeper into said first conductivity type region.

2. The MOS device of claim 1 wherein said silicon or silicon alloy source/drain regions extend above said gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric.

3. The MOS device of claim 1 wherein said gate dielectric layer is thicker beneath outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode.

4. The MOS device of claim 2 wherein said gate dielectric layer is thicker beneath said sidewall spacer and said outside edge of said gate electrode then the gate dielectric layer beneath the center of said gate electrode.

5. The MOS device of claim 1 further comprising a pair of deposited silicon or silicon alloy regions having a first conductivity type formed between said pair of deposited silicon or silicon alloy source/drain regions of said second conductivity type and said first conductivity type region.

6. (Amended) The MOS device of claim 5 wherein the concentration of said deposited silicon or silicon alloy regions having a conductivity type is greater than the concentration of said first conductivity type region.

7. The MOS device of claim 1 wherein said deposited silicon or silicon alloy source/drain regions extend the greatest distance laterally beneath said gate electrode

at an inflection point which occurs of between 50-250Å laterally beneath said gate electrode and at a depth of between 25-200Å beneath said gate dielectric.

8. The MOS device of claim 1 wherein said first conductivity type is n-type conductivity and wherein said second conductivity type is p-type conductivity.

9. The MOS device of claim 1 wherein said first conductivity type is p-type conductivity and wherein said second conductivity type is n-type conductivity.

10. (Amended) The MOS device of claim 1 wherein the concentration of said deposited silicon or silicon alloy source/drain regions of a second conductivity type have a concentration between $1x10^{18}/cm^3 - 3x10^{21}/cm^3$.

11. The MOS device of claim 10 wherein the concentration of said deposited silicon or silicon alloy source/drain regions of a second conductivity type is approximately $1x10^{21}/cm^3$.

12. The MOS device of claim 1 further comprising silicide formed on said deposited silicon or silicon alloy source/drain regions.

13. (Amended) An MOS device comprising:

a gate dielectric formed on a first conductivity type region in a substrate;

a gate electrode formed on said gate dielectric;

a pair of sidewall spacers formed along laterally opposite sidewalls of said gate electrode; and

a pair of deposited silicon or silicon alloy source/drain regions having a second conductivity type formed in said substrate and along opposite sides of said gate

electrode wherein said deposited silicon or silicon alloy extends above the height of said gate dielectric layer wherein the top surface of said deposited silicon or silicon alloy is spaced further from said gate electrode than said silicon or silicon alloy adjacent to said gate dielectric.

14. The MOS device of claim 13 wherein said gate dielectric layer is thicker beneath said outside edges of said gate electrode then the gate dielectric beneath the center of the gate electrode.

15. An MOS device comprising a gate dielectric formed on a first conductivity type region;

a gate electrode formed on said gate dielectric; and

a pair of source/drain regions formed along laterally opposite sides of said gate electrode wherein said gate dielectric layer is thicker beneath the outside edge of said gate electrode then the gate dielectric layer beneath the center of said gate electrode.